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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,439	07/31/2003	Chang-Man Khang	5649-1079	2840

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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,439	KHANG ET AL.	
	Examiner	Art Unit	
	Pho M. Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 2* is/are allowed.

6)☒ Claim(s) *3-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 27 September 2004. The information disclosed therein was considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Ryu et al. (US. 6,404,697).

Regarding claim 3, Ryu et al. in Figures 1 and 3B discloses a data output circuit (300, Figure 3B) comprising:

a plurality of registers (190-0 to190-n in Figure 1; 320-0 to 320-n and 330-0 to 330-n in Figure 3B);

a plurality of register output (190-0 to190-n in Figure 1; 320-0 to 320-n and 330-0 to 330-n in Figure 3B) selection switches (186-0 to 186-n in Figure 1; 312-0 to 312-n and 313-0 to 313-n in Figure 3B) connected to the plurality of registers, pairs of the plurality of register output selection switches being connected by common active region;

a first data group selection switch (350, Figure 3B) connected to the common active region of a first subset of the plurality of register output selection switches (even register 320-0 to 320-n coupled to switch 312-0 to 312-n which is generating to input even data 350);

a second data group selection switch (360, Figure 3B) connected to the common active region of a second subset of the plurality of register output selection switches (odd register 330-0 to 330-n coupled to switch 313-0 to 313-n which is generating to input odd data 360) and

an output driver (370, Figure 3B) is connected to the first data group (350, Figure 3B) and second data group (360, Figure 3B) selection switches.

As described in the specification the CMOS transmission gate coupled to the switch from the input of the multiplexer such as the output line of the multiplexer.

With respected to claim 4, Ryu et al. in Figure 3B disclosed the plurality of register output 190-0 to190-n in Figure 1; 320-0 to 320-n and 330-0 to 330-n in Figure 3B) selection switches (186-0 to 186-n in Figure 1; 312-0 to 312-n and 313-0 to 313-n in

Figure 3B) including a plurality of CMOS transmission gate (multiplexer 340-1 to 340-n in Figure 3B coupled to input switch 312-0 to 312-n and 313-0 to 313-n in Figure 3B).

Regarding claim 5, Ryu et al. in Figures 1 and 3B discloses a data output circuit (300, Figure 3B) comprising:

a plurality of registers (190-0 to190-n in Figure 1; 320-0 to 320-n and 330-0 to 330-n in Figure 3B);

a plurality of register output (190-0 to190-n in Figure 1; 320-0 to 320-n and 330-0 to 330-n in Figure 3B) selection switches (186-0 to 186-n in Figure 1; 312-0 to 312-n and 313-0 to 313-n in Figure 3B) connected to the plurality of registers, pairs of the plurality of register output selection switches being connected by common active region;

a data group selection switch (350, 360, Figure 3B) connected to the plurality of register output selection switches (even register 320-0 to 320-n coupled to switch 312-0 to 312-n which is generating to input even data 350 and odd register 330-0 to 330-n coupled to switch 313-0 to 313-n which is generating to input odd data 360) by a plurality of second wires having second lengths that are shorter than the first length and

an output driver (370, Figure 3B) is connected to the first data group (350, Figure 3B) and second data group (360, Figure 3B) selection switches.

Regarding claim 6, Ryu et al. in Figures 1 and 3B discloses a data output circuit (300, Figure 3B) comprising:

a plurality of registers (190-0 to190-n in Figure 1; 320-0 to 320-n and 330-0 to 330-n in Figure 3B);

a plurality of register output (190-0 to190-n in Figure 1; 320-0 to 320-n and 330-0 to 330-n in Figure 3B) selection switches (186-0 to 186-n in Figure 1; 312-0 to 312-n and 313-0 to 313-n in Figure 3B) connected to the plurality of registers;

a first data group selection switch (350, Figure 3B) connected to the common active region of a first subset of the plurality of register output selection switches via a first line having a first length (even register 320-0 to 320-n coupled to switch 312-0 to 312-n which is generating to input even data 350);

a second data group selection switch (360, Figure 3B) connected to the common active region of a second subset of the plurality of register output selection switches via a second line having a second length that is equal to the first length (odd register 330-0 to 330-n coupled to switch 313-0 to 313-n which is generating to input odd data 360) and

an output driver (370, Figure 3B) is connected to the first data group (350, Figure 3B) and second data group (360, Figure 3B) selection switches.

Regarding claim 7, Ryu et al. in Figures 1 and 3B discloses a data output circuit (300, Figure 3B) comprising:

a plurality of registers (320-0 to 320-n and 330-0 to 330-n in Figure 3B);

a plurality of register output (320-0 to 320-n and 330-0 to 330-n in Figure 3B) selection switches (312-0 to 312-n and 313-0 to 313-n in Figure 3B) connected to the plurality of registers and arranged in a circular configuration;

a plurality of overlap prevention control signal lines, which are connected to pairs of the plurality of register output selection switches (output register 320-0 to 320-n and 330-0 to 330-n coupled to input switches 355-0 to 355-n and switches 365-0 to 365-n for generate the output switch to input 350 and 360);

a data group selection switch (350, 360 Figure 3B) connected to the common active region of a first subset of the plurality of register output selection switches (even register 320-0 to 320-n coupled to switch 312-0 to 312-n which is generating to input even data 350 and odd register 330-0 to 330-n coupled to switch 313-0 to 313-n which is generating to input odd data 360) and

an output driver (370, Figure 3B) is connected to the first data group (350, Figure 3B) and second data group (360, Figure 3B) selection switches.

Allowable Subject Matter

5. Claims 1-2 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "a plurality of third wires having third lengths that are shorter the first lengths, the first and second data group selection switches being disposed approximately the same distance form the first and

second subsets of the plurality of register output selection switch" as claimed in the independent claim 1.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Holst (US. 5,940,334) disclosed the circuit and operation bypass the input write data to the read in place of data transferred to memory device.

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see

http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
March 8, 2005.

VAN THU NGUYEN
PRIMARY EXAMINER